Fig.1

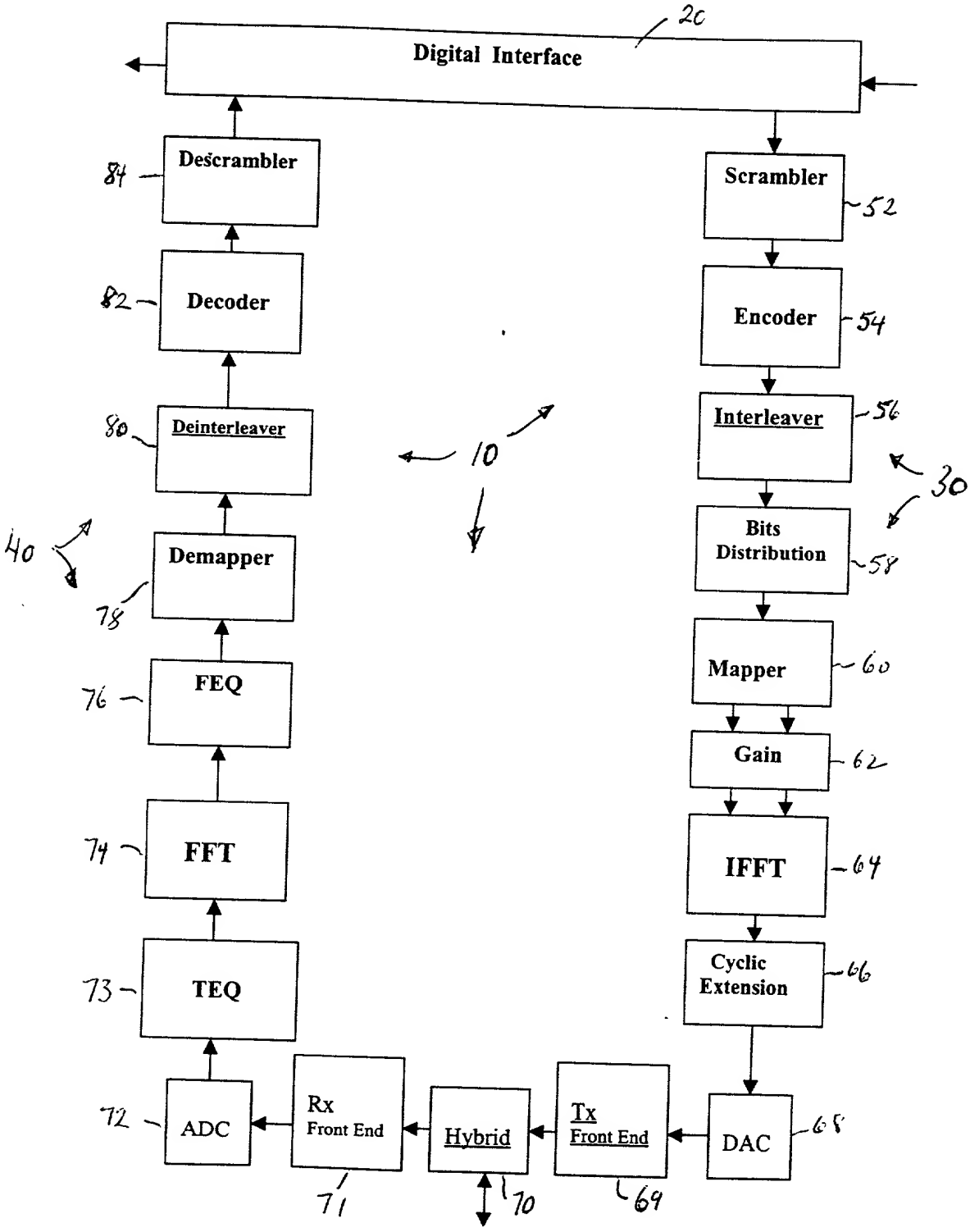

20
Digital Interface
Descrambler
84
Decoder
82
Deinterleaver
80
Demapper
78
FEQ
76
FFT
74
TEQ
73
ADC
72
Rx Front End
71
Hybrid
70
Tx Front End
69
DAC
68
Cyclic Extension
66
IFFT
64
Gain
62
Mapper
60
Bits Distribution
58
Interleaver
56
Encoder
54
Scrambler
52
10
30
40

Fig. 2

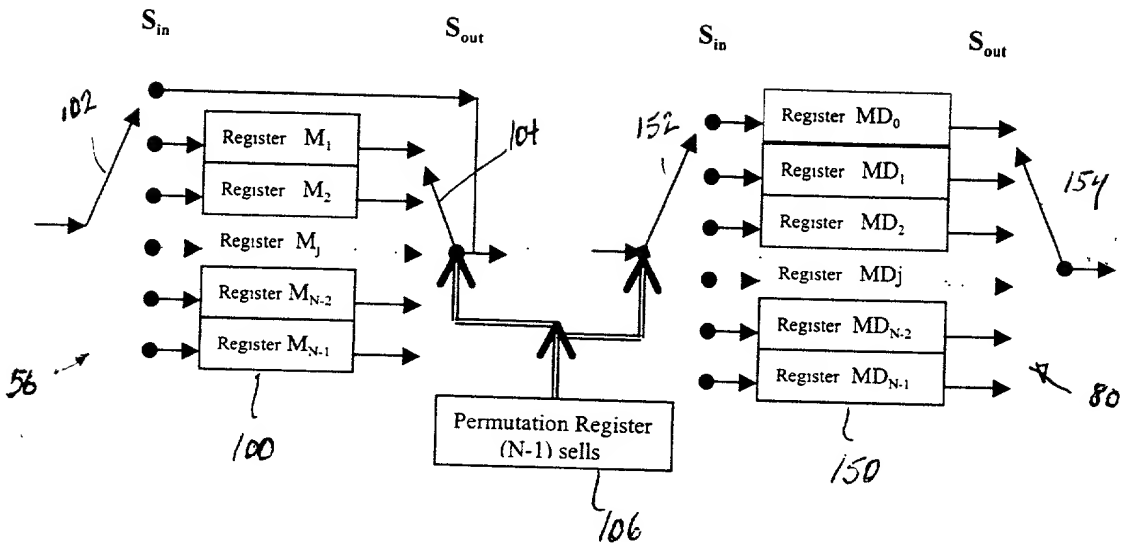

S_{in}
S_{out}
S_{in}
S_{out}
102
Register M_1
Register M_2
Register M_j
Register M_{N-2}
Register M_{N-1}
104
152
Register MD_0
Register MD_1
Register MD_2
Register MDj
Register MD_{N-2}
Register MD_{N-1}
154
56
80
100
Permutation Register
(N-1) sells
106
150

Fig.3

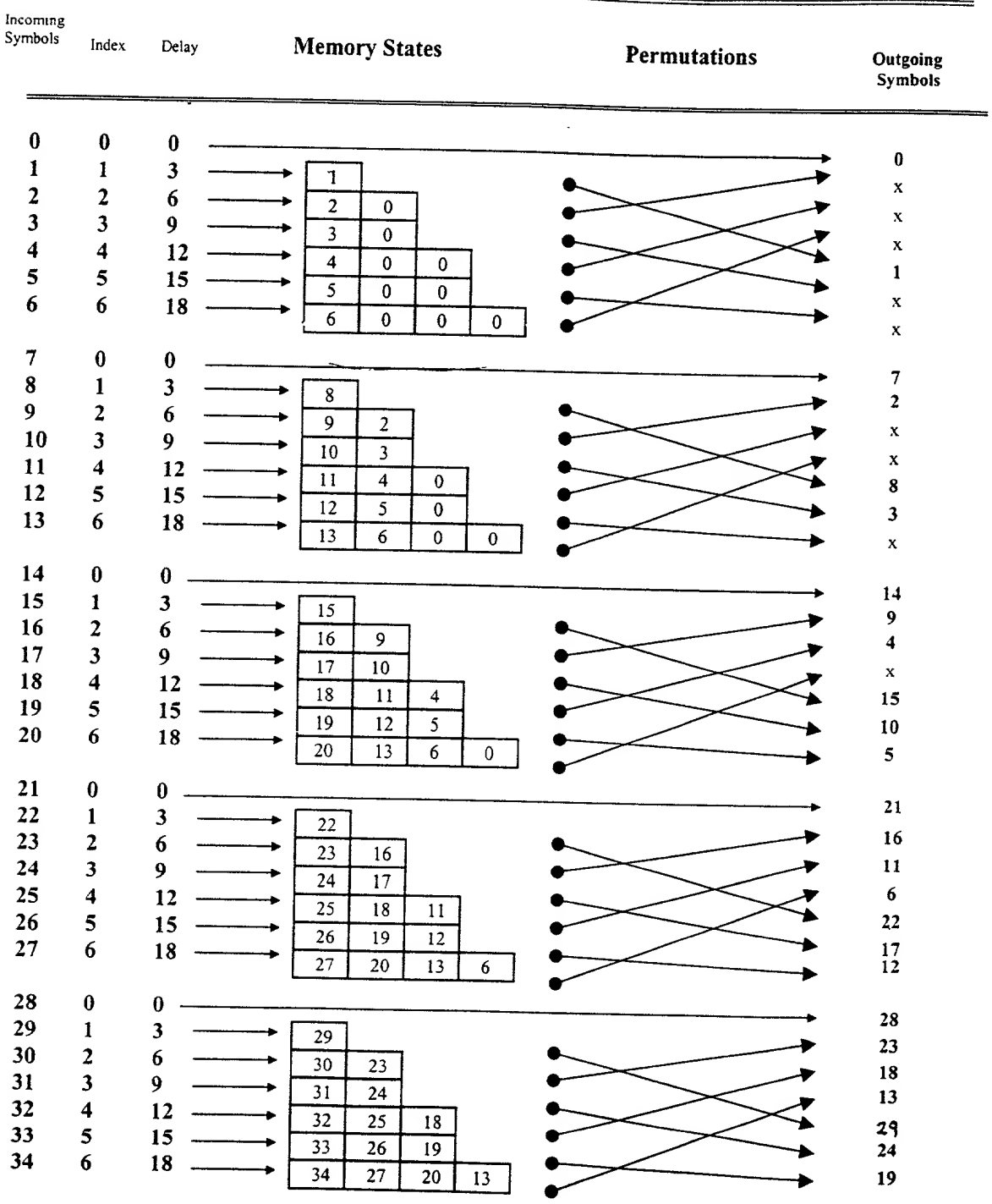

Incoming Symbols
Index
Delay
Memory States
Permutations
Outgoing Symbols
0 0 0
1 1 3
2 2 6
3 3 9
4 4 12
5 5 15
6 6 18
1
2 0
3 0
4 0 0
5 0 0
6 0 0 0
0
x
x
x
1
x
x
7 0 0
8 1 3
9 2 6
10 3 9
11 4 12
12 5 15
13 6 18
8
9 2
10 3
11 4 0
12 5 0
13 6 0 0
7
2
x
x
8
3
x
14 0 0
15 1 3
16 2 6
17 3 9
18 4 12
19 5 15
20 6 18
15
16 9
17 10
18 11 4
19 12 5
20 13 6 0
14
9
4
x
15
10
5
21 0 0
22 1 3
23 2 6
24 3 9
25 4 12
26 5 15
27 6 18
22
23 16
24 17
25 18 11
26 19 12
27 20 13 6
21
16
11
6
22
17
12
28 0 0
29 1 3
30 2 6
31 3 9
32 4 12
33 5 15
34 6 18
29
30 23
31 24
32 25 18
33 26 19
34 27 20 13
28
23
18
13
29
24
19

Fig.4

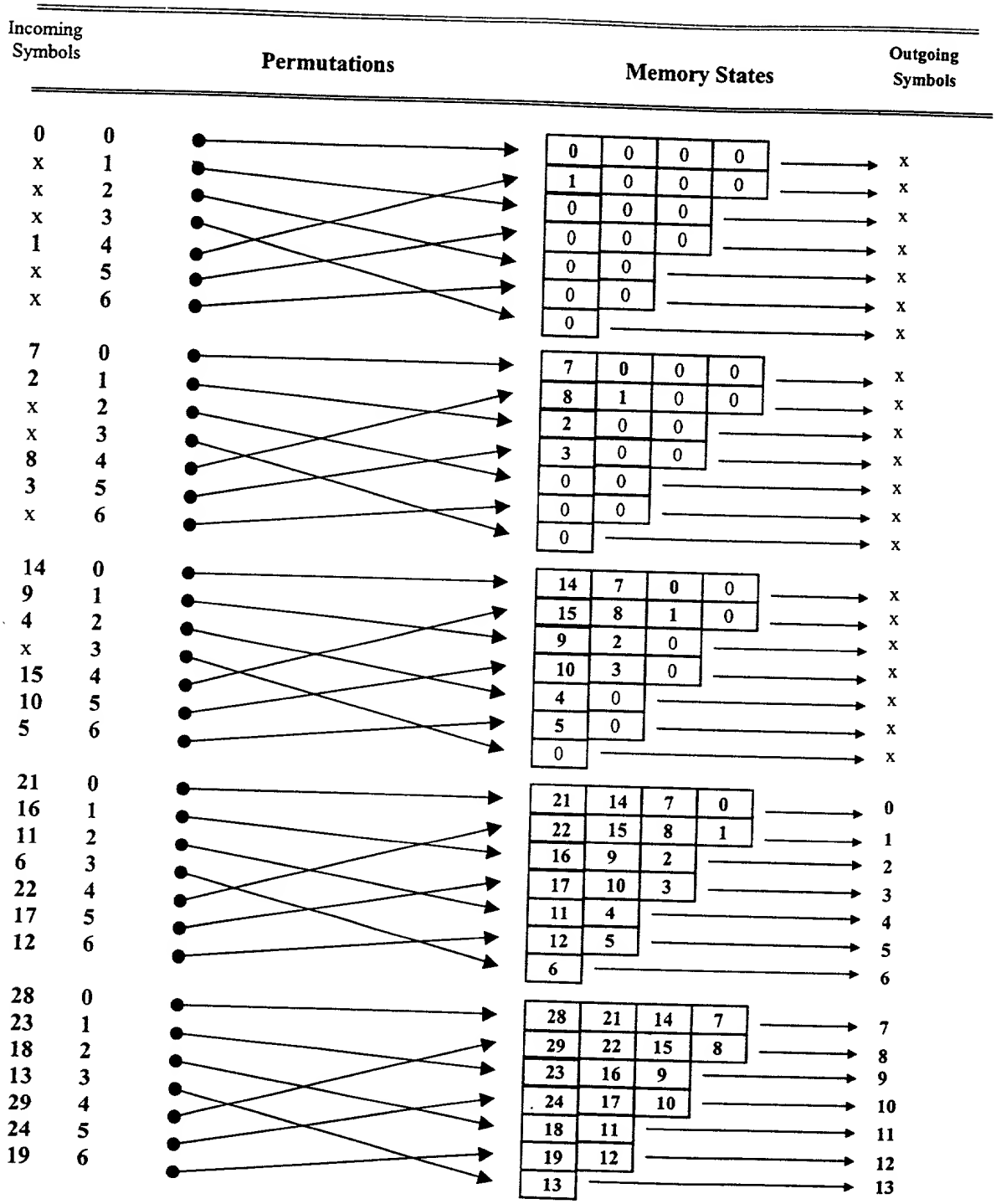

Incoming Symbols
Permutations
Memory States
Outgoing Symbols
0 0
x 1
x 2
x 3
1 4
x 5
x 6
7 0
2 1
x 2
x 3
8 4
3 5
x 6
14 0
9 1
4 2
x 3
15 4
10 5
5 6
21 0
16 1
11 2
6 3
22 4
17 5
12 6
28 0
23 1
18 2
13 3
29 4
24 5
19 6
0 0 0 0
1 0 0 0
0 0 0
0 0 0
0 0
0 0
0
7 0 0 0
8 1 0 0
2 0 0
3 0 0
0 0
0 0
0
14 7 0 0
15 8 1 0
9 2 0
10 3 0
4 0
5 0
0
21 14 7 0
22 15 8 1
16 9 2
17 10 3
11 4
12 5
6
28 21 14 7
29 22 15 8
23 16 9
24 17 10
18 11
19 12
13
x
x
x
x
x
x
x
x
x
x
x
x
x
x
x
x
x
x
x
x
0
1
2
3
4
5
6
7
8
9
10
11
12
13

Fig. 5a

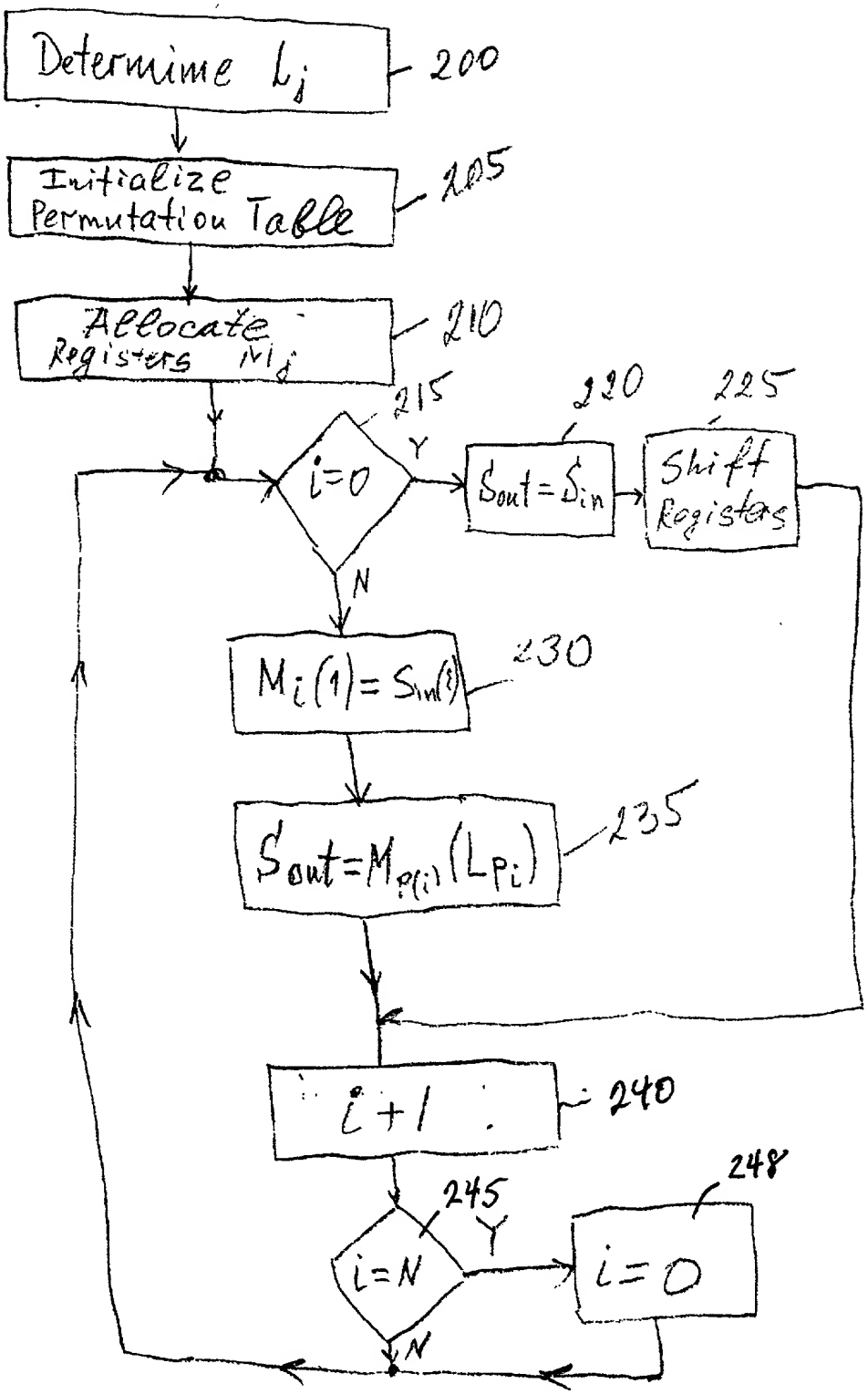
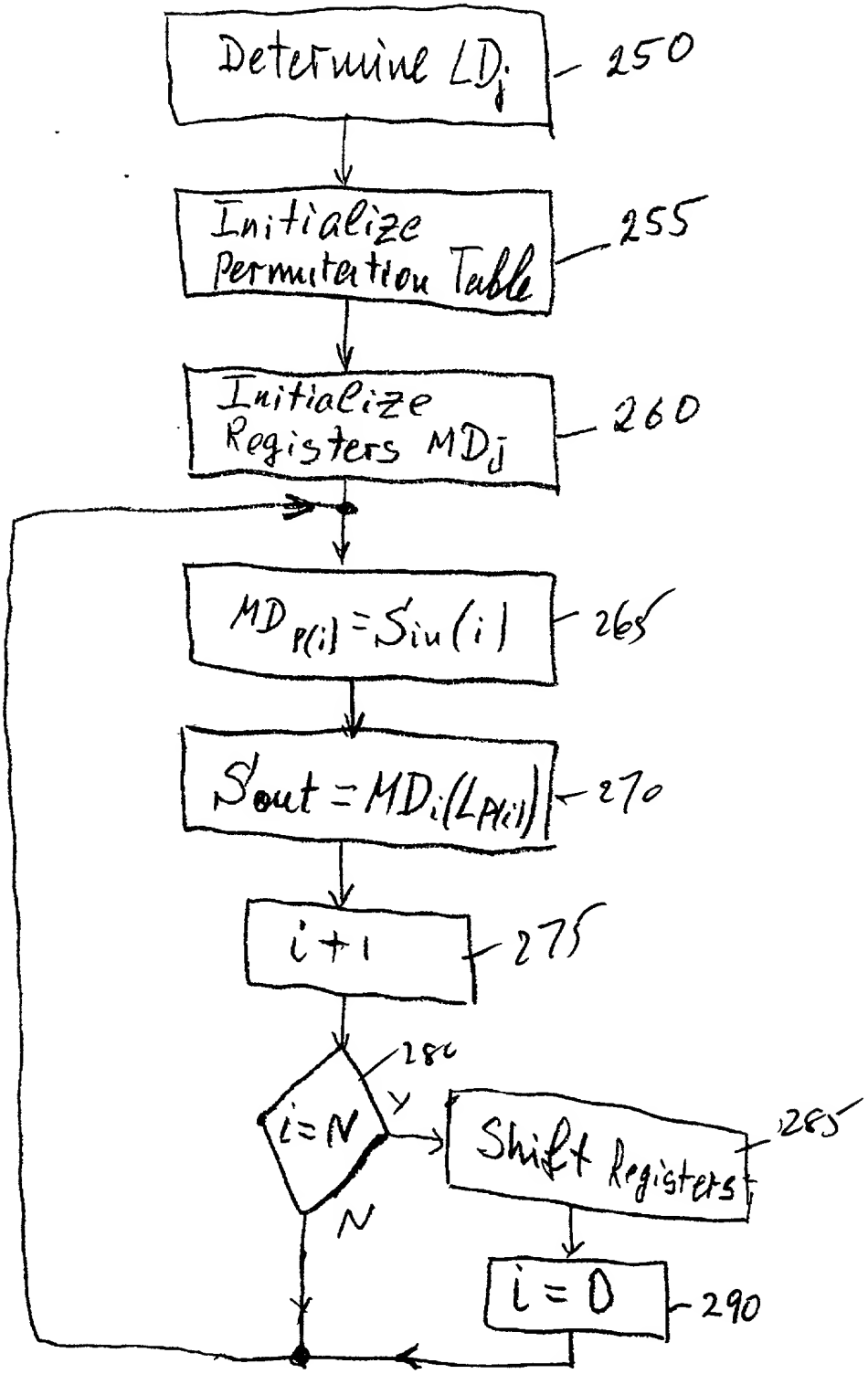

Determine L_j
200
Initialize Permutation Table
205
Allocate Registers M_i
210
215
$i=0$
Y
220
$S_{out}=S_{in}$
225
Shift Registers
N
$M_i(1)=S_{in}(1)$
230
$S_{out}=M_{P(i)}(L_{Pi})$
235
$i+1$
240
245
$i=N$
Y
248
$i=0$
N

Fig. 5b


Determine LD_j
250
Initialize Permutation Table
255
Initialize Registers MD_j
260
$MD_{P(i)} = S_{in}(i)$
265
$S_{out} = MD_i(L_{P(i)})$
270
i+1
275
i=N
280
Y
N
Shift Registers
285
i = 0
290